PVP 20

Code: 20EC6401

II B.Tech - II Semester – Regular Examinations – MAY 2024

DIGITAL ELECTRONICS DESIGN WITH VHDL

(HONORS in ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

Note: 1. This paper contains questions from 5 units of Syllabus. Each unit carries 14 marks and have an internal choice of Questions.
2. All parts of Question must be answered in one place.

BL – Blooms Level CO – Course Outcome

			BL	CO	Max. Marks
UNIT-I					
1	a)	What is VHDL? Write its capabilities.	L2	CO1	7 M
	b)	Explain design flow of digital circuit.	L2	CO1	7 M
OR					
2	a)	Explain various modeling styles of VHDL.	L2	CO2	7 M
	b)	Explain the role and significance of various operators used in VHDL.	L2	CO2	7 M
UNIT-II					
3	a)	How does VHDL handle concurrent and sequential statements? Explain with an example.	L3	CO3	7 M
	b)	Describe entity and architecture of VHDL using 2-input OR gate.	L3	CO1	7 M
OR					

4	a)	Write VHDL code for multiplexer using data flow style of modeling.	L3	CO3	7 M
	b)	What is component instantiation? Write VHDL code for 1-bit full adder using half adder.	L3	CO1	7 M
		UNIT-III			
5	a)	Write syntax of package declaration in VHDL.	L3	CO1	7 M
	b)	Explain package body in VHDL with syntax.	L3	CO3	7 M
		OR			
6	a)	Explain what is meant by test-bench in VHDL and how do you construct a test-bench for 2-input AND gate.	L3	CO3	7 M
	b)	Write the differences between functions and procedures in VHDL.	L3	CO1	7 M
		UNIT-IV			
7	a)	Compare combinational and sequential circuits. Write VHDL code for D-flip-flop using behavioral style of modeling.	L3	CO1	7 M
	b)	Explain state table of SR latch with FSM model representation.	L3	CO3	7 M
		OR			
8	a)	Write VHDL code for 4-bit asynchronous up counter using behavioral modeling.	L3	CO3	7 M
	b)	Explain behavioral modeling using flip-flops with suitable examples.	L3	CO3	7 M

UNIT-V					
9	a)	Explain architecture of PLA with a neat diagram.	L3	CO4	7 M
	b)	Write the differences among PROM, PLA and PLD in terms of fuses, structure, and application.	L3	CO4	7 M
OR					
10	a)	Explain the architecture of Xilinx Xc 4000.	L3	CO4	7 M
	b)	What is the principle of one hot encoding? Compare it with normal encoding with 2-bit counter.	L3	CO4	7 M